UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/697,504	10/30/2003	Takashi Naiki	12844.0050US01	8052

23552 7590 02/03/2005

MERCHANT & GOULD PC
P.O. BOX 2903
MINNEAPOLIS, MN 55402-0903

EXAMINER	
WILLIAMS, ALEXANDER O	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 02/03/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/697,504	NAIKI, TAKASHI	
	Examiner	Art Unit	
	Alexander O Williams	2826	

-- The MAILING DATE f this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 November 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 2* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 2* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 November 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Serial Number: 10/697504 Attorney's Docket #: 12844.0050US01
Filing Date: 10/30/2003; claimed foreign priority to 10/31/2002

Applicant: Naiki

Examiner: Alexander Williams

Applicant's Amendment filed 11/1/04 has been acknowledged.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1 and 2 are rejected under 35 U.S.C. § 102(b) as being anticipated by Mori et al. (Japan Patent # 2001-35872).

1. Mori et al. (figures 1 to 12) specifically figures 1 and 2 show a semiconductor integrated circuit device **1** comprising a semiconductor substrate **30** and a

semiconductor chip **20** having bumps **22**, which are for electrically connecting by face down bonding with a terminal section on a surface of the semiconductor substrate, said semiconductor integrated circuit device further comprising: facedown bonding dummy bumps **23** which are connected non-electrically and disposed in a vicinity of one or more corner sections of four corners of a semiconductor chip, wherein said bumps are arranged along and spaced from a peripheral edge of the semiconductor integrated circuit device and an area of each of said facedown bonding dummy bumps projected onto a chip is larger than that of the area of each said facedown bonding bumps, the height of the facedown dummy bonding bumps being the same as the height of the facedown bonding bumps.

2. The semiconductor integrated circuit device according to claim 1, Mori et al. show wherein said dummy bumps **23** act as shock absorbing members for alleviating load stress due to the facedown bonding, and are overlapping with a wiring with at least one insulating film being interposed in-between.

PAT-NO: JP02001035872A

TITLE: MOUNTING STRUCTURE AND BUMP STRUCTURE OF SEMICONDUCTOR DEVICE

PUBN-DATE: February 9, 2001

INVENTOR-INFORMATION:

NAME	COUNTRY
MORI, SHIGERU	N/A
NARUI, JOSHI	N/A
ISHII, TSUGUHISA	N/A
INOUE, NORIHIRO	N/A

ASSIGNEE-INFORMATION:

NAME	COUNTRY
FUJITSU TEN LTD	N/A

APPL-NO: JP11204789

APPL-DATE: July 19, 1999

INT-CL (IPC): H01L021/60

ABSTRACT:

PROBLEM TO BE SOLVED: To prevent cracking of a bump at the solder joint of the electrode of a semiconductor device and a connection pattern formed on a substrate by arranging bumps densely at four corners of the semiconductor device as compared with other parts.

SOLUTION: A semiconductor device 20 is a face down mounting chip wherein an electronic circuit is formed on the lower surface of a silicon substrate and electrodes 21 for connecting the electronic circuit with a substrate 30 are formed at the bottom face art along with a pattern 24. Bumps 22 for connection with a connection pattern 31 formed on the substrate 30 are formed on the electrodes 21 and a pattern 31 for connection with the electrodes 21, a pattern 32 for connection with dummy bumps 23 at four corners of the semiconductor device 20 and a circuit for connection with other electronic parts are formed oppositely to the bumps 22. According to the structure, connection strength can be enhanced at four corners of the semiconductor device 20 and thermal stress being applied to bumps 22 in the vicinity of four corners can be lessened.

Claims 1 and 2 are rejected under 35 U.S.C. § 102(e) as being anticipated by Nishikawa et al. (U.S. Patent Application Publication # 2003/0092326 A1).
!. Nishikawa et al. (figures 7A-7C) specifically figures 7C show a semiconductor integrated circuit device comprising a semiconductor substrate **26** and a semiconductor chip **21**having bumps **3**, which are for electrically connecting by face down bonding with a terminal section on a surface of the semiconductor substrate, said semiconductor integrated circuit device further comprising: facedown bonding dummy bumps **5** which are connected non-electrically and disposed in a vicinity of one or more corner sections of four corners of a semiconductor chip, wherein said bumps are arranged along and spaced from a peripheral edge of the semiconductor integrated circuit device and an area of each of said facedown bonding dummy bumps projected onto a chip is larger than that of the area of each said facedown bonding bumps, the height of the facedown dummy bonding bumps being the same as the height of the facedown bonding bumps.
2. The semiconductor integrated circuit device according to claim 1, (Japan Patent # 4-94732) wherein said dummy bumps **5** act as shock absorbing members for alleviating

load stress due to the facedown bonding, and are overlapping with a wiring with at least one insulating film being interposed in-between.

DOCUMENT-IDENTIFIER: US 20030092326 A1

TITLE: Electronic parts packaging method and electronic parts package

Detail Description Paragraph - DETX (37):

[0221] In the first embodiment and the second embodiment, an array of bumps 2, . . . , 2; 12, . . . , 12 are provided in each of the vicinities of side verges of the four sides of a square or rectangular IC chip 1, 11, while dummy bumps 3, 13 are disposed at sites at which an array of bumps is lacking in the vicinities of side verges of the individual sides. However, this is not limitative. For example, in the third embodiment, as shown in FIGS. 7A and 7B, a bonding surface of a square IC chip 21 has an array of bumps 22, . . . , 22 in each of vicinities of side verges of the four sides except the vicinities of its four corner portions, and dummy bumps 23 are formed as an example of a bonding-material flow regulating member in each of vicinities of the four corner portions of the bonding surface of the IC chip 21, that is, at portions where no bumps are originally provided, so that the flow regulation of a bonding material 25 is performed by the dummy bumps 23.

Detail Description Paragraph - DETX (39):

[0223] In order to prevent such deteriorations of the bonding power and the sealing power, in the third embodiment, prior to the bonding material feeding step, as shown in FIGS. 7A and 7B, a singularity or plurality of dummy bumps 23 are disposed in vicinities 123 of corner portions of the square IC chip 21 where the bumps 22 are absent. In this connection, the expression that a singularity or plurality of dummy bumps 23 are disposed in vicinities 123 of corner portions means that when extension lines L1 and L2 of array lines of the bumps 22, . . . , 22 in the vicinities of side verges of the bonding surface of the IC chip 21 cross each other generally at 90.degree. at a corner portion of the bonding surface of the IC chip 21 as shown in FIG. 26, the dummy bumps are disposed in a region R1 outside the crossing region as indicated by 23A and 23B or in a region R2 enclosed by reference lines L3 and L4, which pass the bumps 22 closest to the corner portion in their respective array lines and cross perpendicularly to the extension lines L1 and

L2, respectively, as indicated by 23A, 23B and 23C. Consequently, a bump is present also in the vicinity of each corner portion of the square IC chip 21, resulting in a state that the bumps 22, . . . , 22 or the dummy bumps 23, . . . , 23 are arrayed generally uniformly in the vicinities of all the side verges and corner portions.

Detail Description Paragraph - DETX (43):

[0227] Next, at the final compression-bonding step, a pressurizing member 28 is brought into contact with the IC chip 21 so that a pressurizing force acts from the pressurizing member 28 toward the base 30, on which the circuit board 26 having the IC chip 21 laid thereon with the bonding material 25 interposed therebetween is placed, and moreover heat of a heater contained in the pressurizing member 28 is transferred from the pressurizing member 28 to the IC chip 21. As a result of this, by a specified pressurizing force being exerted under application of a specified temperature, the bonding surface of the IC chip 21 is pressed against the IC chip bonding region 26a of the circuit board 26, causing the bumps 22 on the individual electrodes 24 of the bonding surface of the IC chip 21 to come into contact with the individual electrodes 27 within the IC chip bonding region 26a of the circuit board 26. In this state, the bonding material 25 between the bonding surface of the IC chip 21 and the IC chip bonding region 26a of the circuit board 26 tends to be pressed out from central portions toward peripheral portions of the bonding surface of the IC chip 21. In this connection, since the dummy bumps 23 are disposed at positions where the bumps 22 are lacking, i.e. vicinities of the corner portions, as described above, the bumps 22, . . . , 22 and the dummy bumps 23 are disposed generally equidistantly in the vicinities of the individual corner portions of the bonding surface of the IC chip 21, as they are in the vicinities of side verges of all the sides. Therefore, flow of the bonding material 25 from the central portions toward the peripheral portions is regulated similarly in the vicinities of the side verges of the individual sides as well as in the corner portions as shown by arrows in FIG. 8, so that the bonding material 25 can be prevented from flowing nonuniformly. Thus, the bonding material 25 is cured by the heat, while being held generally uniformly distributed, over at least the whole bonding surface of the IC chip 21, achieving the manufacture of the IC chip-mounted unit. That is, in this final compression-bonding step, nonuniform pressing out of the bonding material 25 from the central portion to the peripheral portions of the bonding surface of the IC chip 21 in the compression-bonding can

be regulated by the dummy bumps 23, . . . , 23 provided on the IC chip 21.

Claims 1 and 2 are rejected under 35 U.S.C. § 102(e) as being anticipated by Kimura et al. (U.S. Patent Application Publication # 2003/0060035 A1).

1. Kimura et al. (figures 1 to 16) specifically figures 5 and 7 show a semiconductor integrated circuit device comprising a semiconductor substrate **4** and a semiconductor chip **1** having bumps **2**, which are for electrically connecting by face down bonding with a terminal section on a surface of the semiconductor substrate, said semiconductor integrated circuit device further comprising: facedown bonding dummy bumps **3** which are connected non-electrically and disposed in a vicinity of one or more corner sections of four corners of a semiconductor chip, wherein said bumps are arranged along and spaced from a peripheral edge of the semiconductor integrated circuit device and an area of each of said facedown bonding dummy bumps projected onto a chip is larger than that of the area of each said facedown bonding bumps, the height of the facedown dummy bonding bumps being the same as the height of the facedown bonding bumps.

2. The semiconductor integrated circuit device according to claim 1, (Japan Patent # 4-94732) wherein said dummy bumps **3** act as shock absorbing members for alleviating load stress due to the facedown bonding, and are overlapping with a wiring with at least one insulating film being interposed in-between.

DOCUMENT-IDENTIFIER: US 20030060035 A1

TITLE: Semiconductor device

Detail Description Paragraph - DETX (6):
[0027] A second embodiment of the invention will now be explained. In the second embodiment, as shown in FIG. 2, the dummy bumps 3 are provided only at the corners of the semiconductor chip 1. That is, the dummy bump 3 is provided at a point-symmetric vacant position of a function bump 2 which does not establish the point-symmetry in the corner region of the semiconductor chip 1.

Detail Description Paragraph - DETX (7):
[0028] According to the second embodiment, inconvenience that one of opposed corner regions of the semiconductor chip 1 is largely bent locally is avoided, and the connection force of the

function bump 2 is enhanced. Further, even when the function bump 2 exists in an inner region of the semiconductor chip 1 as shown in FIG. 1, since the disposition position of the dummy bump 3 is limited to the corner region, there is a merit that the number of dispositions of the dummy bumps 3 is reduced.

Detail Description Paragraph - DETX (8):
[0029] In this second embodiment, when two sides of the semiconductor chip 1 are respectively defined as side D and side E, a size of the corner region is set to (D/3).times.(E/3) This size of the region may appropriately be changed in accordance with arrangement density or the like of the function bumps 2 and dummy bumps 3.

Detail Description Paragraph - DETX (10):
[0031] According to the third embodiment, the dummy bumps 3 are disposed at least at positions close to the corners of the semiconductor chip 1. Therefore, even if the corner portion of the semiconductor chip 1 is bent in the vertical direction, a connection failure is generated only in the dummy bump 3. That is, connection failure in the function bump 2 is avoided.

Detail Description Paragraph - DETX (20):
[0041] According to the sixth embodiment, like the case in which the dummy bumps 3 are provided, an excellent connection force of the function bump 2 located at the corner of the semiconductor chip 1 can be secured.

This rejection remain outstand since there was no translation submitted.

Claims 1 and 2 are rejected under 35 U.S.C. § 102(e) as being anticipated by Yagi et al. (Japan Patent # 2003-282812).

1. Yagi et al. (figures 1a to 5b) specifically figure 1 a show a semiconductor integrated circuit device comprising a semiconductor substrate and a semiconductor chip having bumps **11**, which are used for electrically connecting by face down bonding and provided in a terminal section on a surface of a semiconductor substrate thereof, said semiconductor integrated circuit device further comprising: facedown bonding dummy bumps **15** which are connected non-electrically and disposed in a vicinity of one or more corner sections of four corners of a semiconductor chip, wherein an area of each of said facedown bonding dummy bumps projected onto a chip is larger than that of the area of each said facedown bonding bumps.

2. The semiconductor integrated circuit device according to claim 1, Yago et al. show wherein said dummy bumps are functioning as shock absorbing members for alleviating load stress due to the facedown bonding, and are not electrically connected to a wiring of which part is disposed to be overlapped to said facedown bonding dummy bumps with at least one insulating film being interposed in-between.

Applicant cannot rely upon the foreign priority papers to overcome this rejection because a translation of said papers has not been made of record in accordance with 37 CFR 1.55. See MPEP § 201.15.

Response

Applicant's arguments filed 11/24/04 have been fully considered, but are moot in view of the new grounds of rejections detailed above.

The insertion of Applicant's additional claimed language, for example, "in claims 1 and 2" cause for further search and consideration to make this action final.

Applicant's amendment necessitated the new grounds of rejection. Accordingly, **THIS ACTION IS MADE FINAL**. See M.P.E.P. § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 C.F.R. § 1.136(a).

A SHORTENED STATUTORY PERIOD FOR RESPONSE TO THIS FINAL ACTION IS SET TO EXPIRE THREE MONTHS FROM THE DATE OF THIS ACTION. IN THE EVENT A FIRST RESPONSE IS FILED WITHIN TWO MONTHS OF THE MAILING DATE OF THIS FINAL ACTION AND THE ADVISORY ACTION IS NOT MAILED UNTIL AFTER THE END OF THE THREE-MONTH SHORTENED STATUTORY PERIOD, THEN THE SHORTENED STATUTORY PERIOD WILL EXPIRE ON THE DATE THE ADVISORY ACTION IS MAILED, AND ANY EXTENSION FEE PURSUANT TO 37 C.F.R. § 1.136(a) WILL BE CALCULATED FROM THE MAILING DATE OF THE ADVISORY ACTION. IN NO EVENT WILL THE STATUTORY

PERIOD FOR RESPONSE EXPIRE LATER THAN SIX MONTHS FROM THE DATE OF THIS FINAL ACTION.

The following references are cited as of interest to this application, but not applied at this time.

Field of Search	Date
U.S. Class and subclass: 257/737,738,734,778,780,781,784,772,775	6/28/04 2/1/05
Other Documentation: foreign patents and literature in 257/737,738,734,778,780,781,784,772,775	6/28/04 2/1/05
Electronic data base(s): U.S. Patents EAST	6/28/04 2/1/05

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander O Williams whose telephone number is (571) 272 1924. The examiner can normally be reached on M-F 6:30-7:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272 1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AOW
2/1/05

Primary Patent Examiner
Alexander O. Williams